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**Claim 11 (Currently Amended)** A complementary metal oxide semiconductor (CMOS) structure comprising:

a gate region formed on a surface of a semiconductor substrate, said gate including an dielectric layer formed on exposed vertical sidewalls thereof and a substrate surface;

a vertical nitride spacer element formed on each said vertical sidewall of said gate stack overlying said dielectric layer, whereby a portion of said dielectric layer underlies said vertical nitride spacer and above [[a]] said substrate surface such that an edge of said portion of said dielectric layer underlying said vertical nitride spacer is aligned with an outer edge of said vertical nitride spacer element;

a nitride plug formed over said gate stack, vertical nitride spacer elements and said edge of said portion of said dielectric layer underlying said vertical nitride spacer underlying dielectric-layer portion, said nitride plug encapsulating and sealing said underlying dielectric layer;

and,

silicide contacts formed on other portions of said semiconductor substrate adjacent said patterned gate region, for contact with drain and source regions formed in said semiconductor substrate.

**Claim 13. (Original)** The complementary metal oxide semiconductor (CMOS) structure as claimed in Claim 11, wherein an edge of said portion of said dielectric layer underlying said vertical nitride spacer is pulled back out of alignment with a vertical edge of said vertical nitride spacer element.

**Claim 14. (Original)** The complementary metal oxide semiconductor (CMOS) structure as claimed in Claim 11, wherein said semiconductor substrate is comprised of Si, Ge, SiGe, GaAs, InAs, InP, Si/Si, Si/SiGe, or silicon-on-insulators.

**Claim 15. (Original)** The complementary metal oxide semiconductor (CMOS) structure as claimed in Claim 14, wherein said semiconductor substrate is comprised of Si or silicon-on-insulator.

**Claim 16. (Original)** The CMOS structure of Claim 11, wherein said patterned gate region includes at least a gate dielectric and a gate conductor material.

**Claim 17. (Original)** The CMOS structure of Claim 16, wherein said gate dielectric is comprised of an oxide, a nitride, an oxynitride, or combinations and multilayers thereof.

**Claim 18. (Original)** The CMOS structure of Claim 16, wherein said gate dielectric is an oxide selected from the group consisting of  $\text{SiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$ .

**Claim 19. (Original)** The CMOS structure of Claim 16, wherein said gate material is comprised of polysilicon, amorphous silicon, elemental metals that are conductive, alloys of elemental metals that are conductive, silicides or nitrides of elemental metals that are conductive or any combination thereof.

**Claim 20. (Original)** The CMOS structure of Claim 19, wherein said gate material is comprised of polysilicon or amorphous silicon.